## *Remarks*

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendment, claims 2, 5, 7, 9-11, and 19-21 are pending in the application, with claims 2, 5, 19, and 20 being the independent claims. Claims 6 and 8 are sought to be canceled without prejudice to or disclaimer of the subject matter therein. Claims 2, 5, 9-11, 19, and 20 are sought to be amended. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Based on the above amendment and the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding rejections and that they be withdrawn.

### *Rejections Under 35 U.S.C. § 102*

#### *Itakura*

The Office Action rejected claims 2, 5, 6, 8-11, and 19-21 as being anticipated by U.S. Patent No. 5,608,352 to Itakura (hereinafter " Itakura"). (*See* Office Action at p. 2.)

Regarding claims 6 and 8, Applicants have canceled these claims without prejudice to or disclaimer of the subject matter therein, rendering these rejections moot.

Regarding claims 2, 5, 9-11, and 19-21, Applicants respectfully traverse these rejections.

The Office Action, at page two, states:

> Fig. 18 of Itakura discloses an amplifier comprising: inputs INPUT1, INPUT2 that receive differential signals can be read as a differential input; transistors T1, T2 can be read as a first differential pair; transistors T3, T4 can

be read as a second differential pair; output at OUTPUT1, OUTPUT2 can be read as a differential output; level shift circuits LS1 can be read as a differential offset circuit; transistors T5, T6 can be read as a differential switch circuit or a comparison between a common mode voltage of the input signal and a reference voltage to select a subcomponent from a plurality of subcomponents (see spec. col. 4, line 53 - col. 5, line 9); $V_{CC}$ can be read as a first power supply voltage; ground can be read as a second power supply voltage.

Amended independent claim 2 recites (emphasis added):

A differential amplifier, comprising:
a differential input capable of receiving a differential signal;
a first differential pair coupled to said differential input;
a second differential pair, coupled to said differential input, and connected in parallel with said first differential pair at a differential output;
a differential offset circuit, coupled ***within a differential signal path*** between said differential input and said second differential pair, and capable of level shifting said differential signal from a first level to a second level; and
a differential switch circuit, coupled to said first differential pair and said second differential pair, and capable of controlling a first current flow to said first differential pair and a second current flow to said second differential pair.

Itakura does not disclose, teach, or suggest a differential amplifier having a differential input, a first differential pair, a second differential pair, and a differential offset circuit, in which the differential offset circuit is coupled within a differential signal path between the differential input and the second differential pair. Therefore, Itakura does not anticipate claim 2.

Amended independent claim 5 recites (emphasis added):

A differential amplifier, comprising:
a differential input capable of receiving a differential signal;
a first differential pair coupled to said differential input;
a second differential pair, coupled to said differential input, and connected in parallel with said first differential pair at a differential output;
a differential switch circuit, coupled ***outside a differential signal path*** to said first differential pair and ***outside said differential signal path*** to said second differential pair, and capable of controlling a first current flow to said first differential pair and a second current flow to said second differential pair; and

> a differential offset circuit, coupled between said differential input and said second differential pair, and capable of level shifting said differential input signal from a first level to a second level.

Itakura does not disclose, teach, or suggest a differential amplifier having a differential input, a first differential pair, a second differential pair, and a differential switch circuit, in which the differential switch circuit is coupled outside a differential signal path to the first differential pair and outside the differential signal path to the second differential pair. Therefore, Itakura does not anticipate claim 5. Because claims 7 and 9-11 depend upon claim 5 and because of the additional distinctive features of each of claims 7 and 9-11, these claims are also not anticipated by Itakura.

Amended independent claim 19 recites (emphasis added):

> A method of extending an input signal range of a component that receives the input signal, comprising the steps of:
> (1) level shifting a voltage of the input signal;
> (2) processing said level shifted voltage within the component; and
> (3) selecting a subcomponent, from a plurality of subcomponents within the component, to process said level shifted voltage;
> ***wherein the level shifting is performed by a first circuit within a signal path of the input signal; and***
> ***wherein the selecting is performed by a second circuit outside the signal path of the input signal.***

Independent claim 20 has been amended in a similar manner. As explained above, Itakura does not disclose, teach, or suggest a method of extending an input signal range of a component that receives an input signal, in which level shifting a voltage of the input signal is performed by a first circuit within a signal path of the input signal and selecting a subcomponent to process the level shifted voltage is performed by a second circuit outside the signal path of the input signal. Therefore, Itakura does not anticipate claims 19 or 20. Because claim 21 depends upon claim 19 and because of the additional distinctive features claim 21, claim 21 is also not anticipated by Itakura.

Accordingly, Applicants respectfully request that the Examiner reconsider and remove her rejections of claims 2, 5, 9-11, and 19-21under 35 U.S.C. § 102(b) with respect to Itakura.

***Ide***

The Office Action rejected claims 5, 7, and 8 as being anticipated by U.S. Patent No. 5,955,921 to Ide *et al.* (hereinafter " Ide"). (*See* Office Action at p. 2.)

Regarding claim 8, Applicants have canceled this claim without prejudice to or disclaimer of the subject matter therein, rendering this rejection moot.

Regarding claims 5 and 7, Applicants respectfully traverse these rejections.

The Office Action, at pages two and three, states:

> Fig. 8 of Ide et al. discloses a circuit comprising: inputs that received differential signals INPUT+, INPUT- can be read as a differential input; FETs 37A, 37B can be read as a first differential pair; FETs 38A, 38B can be read as a second differential pair; output at OUTPUT+, OUTPUT- can be read as a differential output; transistors 39A, 39B can be read as a differential switch circuit; constant current source 40 can be read as a current source; upper power supply voltage connects to resistors 36A, 36B can be read as a first power supply voltage; ground can be read as a second power supply voltage.

Amended independent claim 5 recites (emphasis added):

> A differential amplifier, comprising:
>
> a differential input capable of receiving a differential signal;
>
> a first differential pair coupled to said differential input;
>
> a second differential pair, coupled to said differential input, and connected in parallel with said first differential pair at a differential output;
>
> a differential switch circuit, coupled outside a differential signal path to said first differential pair and outside said differential signal path to said second differential pair, and capable of controlling a first current flow to said first differential pair and a second current flow to said second differential pair; and

***a differential offset circuit, coupled between said differential input and said second differential pair, and capable of level shifting said differential input signal from a first level to a second level.***

Ide does not disclose, teach, or suggest a differential amplifier having a differential input, a first differential pair, a second differential pair, and a differential offset circuit, in which the differential offset circuit is coupled between the differential input and the second differential pair. Therefore, Ide does not anticipate claim 5. Because claim 7 depends upon claim 5 and because of the additional distinctive features of claim 7, claim 7 is also not anticipated by Ide. Accordingly, Applicants respectfully request that the Examiner reconsider and remove her rejections of claims 5 and 7 under 35 U.S.C. § 102(b) with respect to Ide.

## *Conclusion*

All of the stated grounds of rejection have been properly traversed or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

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